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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/724,866	12/02/2003	Seijiro Tomita	031304	1613

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EXAMINER	
RAO, ANAND SHASHIKANT	
ART UNIT	**PAPER NUMBER**
2621	

MAIL DATE	DELIVERY MODE
08/21/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/724,866	TOMITA, SEIJIRO	
	Examiner	Art Unit	
	Andy S. Rao	2621	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12/2/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamazaki.

Yamazaki discloses a stereoscopic video image display apparatus (Yamazaki: figure 2; column 1, lines 10-25) including an image pick-up device for picking up the image of an object to be observed (Yamazaki: column 2, lines 45-55), a display device for displaying the video image which is picked up by said pick-up device and a stereoscopic video signal processing circuitry for processing (Yamazaki: column 3, lines 50-67) and converting the video signal output from said image pick-up device into a signal which can be displayed on said display device (Yamazaki: column 4, lines 25-35), characterized in that said image pick-up device comprises right and left-eye image pick-up elements which pick up right and left-eye video images, respectively, (Yamazaki: figure 2, element 3a and 3b); and in that said stereoscopic video signal processing circuitry comprises a video signal correction circuit which alternately

corrects the right and left-eye video signals and a first switch for alternately switching the right and left-eye video signals (Yamazaki: figure 2, element S7) to said video signal correction circuit (Yamazaki: column 3, lines 9-47), as in claim 1.

Regarding claim 2, Yamazaki discloses that said display device comprises a right and left-eye display elements for displaying the right and left-eye video images, respectively (Yamazaki: figure 2, elements 19 and 20); and in that said stereoscopic video signal processing circuitry comprises a second switch for separating said video signal output from said video signal correction circuit into right and left-eye video signals for supplying them to said right and left-eye display elements, respectively (Yamazaki: figure 2, element S8), as in the claim.

Regarding claims 3-4, Yamazaki discloses that said first and second switches switch the right and left-eye video signals in accordance with dot synchronization timing, horizontal synchronization timing or vertical synchronization timing of the video signal (Yamazaki: column 7, lines 67-67; column 8, lines 1-20), as in the claims

Regarding claim 5, Yamazaki discloses that said video image correction circuit comprises an amplifier having a variable gain or an attenuator having a variable attenuation (Yamazaki: column 3, lines 20-31), so that the difference between the levels of the right and left-eye video signals is corrected by adjusting said gain and attenuation depending upon the output level of said video signal correction circuit (Yamazaki: column 3, lines 40-50), as in the claim.

Regarding claim 6, Yamazaki discloses said video signal correction circuit includes a level shift circuit which is capable of shifting the direct current level of an input signal (Yamazaki: column 2, lines 60-67: luminance level is DC level in an image), so that the difference between the levels of the right and left-eye video signals is corrected by adjusting the

direct current level of said input signal depending upon the direct current level of the output signal of said video signal correction circuit (Yamazaki: column 3, lines 19-30), as in the claim.

Regarding claim 7, Yamazaki discloses that said video signal correction circuit corrects the difference between the right and left-eye video signals by correcting the pedestal levels of both video signals and/or video signal level (Yamazaki: column 3, lines 37-47), as in the claim.

Regarding claim 8, Yamazaki discloses that said video signal correction circuit comprises a color correction circuit, which is capable of adjusting the tonality of the video signal to correct the difference between the tonality of the right and left-eye video signals (Yamazaki: column 3, lines 30-37), as in the claim.

Regarding claim 9, Yamazaki discloses that said stereoscopic video signal processing circuit operates to cause said first switch to pass one of the right and left-eye video signals and operates to alternately switch said second switch (Yamazaki: column 5, lines 30-50; figure 2, elements S7 and S8), as in the claim.

Yamazaki discloses stereoscopic video signal processing circuitry for processing and converting right and left-eye video signals (Yamazaki: figure 2, elements 6, 17a, 17b; column 3, liens 45-68; column 4, lines 1-10) from right and left-eye image pick-up elements into a signal (Yamazaki: figure 2, elements 3a and 3b) which can be displayed on a display device for displaying a stereoscopic video image (Yamazaki: column 1, lines 10-20; figure 2, elements 19 and 20), characterized in that said stereoscopic video signal processing circuitry comprises a video signal correction circuit which alternately corrects the right and left-eye video signals (Yamazaki: column 3, lines 67; column 4, lines 1-2) and a first switch for alternately switching

the right and left-eye video signals to said video signal correction circuit (Yamazaki: column 5, lines 30-45; figure 2, element S7), as in claim 10.

Regarding claim 11, Yamazaki discloses that said stereoscopic video signal processing circuitry comprises a second switch for separating said video signal output from said video signal correction circuit into right and left-eye video signals for supplying them to said right and left-eye display elements, respectively (Yamazaki: figure 2, element S8), as in the claim.

Regarding claim 12, Yamazaki discloses that said stereoscopic video signal processing circuitry has said first and second switches switch the right and left-eye video signals in accordance with dot synchronization timing, horizontal synchronization timing or vertical synchronization timing of the video signal (Yamazaki: column 7, lines 65—67; column 8, lines 1-20), as in the claim.

Regarding claim 13, Yamazaki discloses that said stereoscopic video signal processing circuitry is characterized in that said video image correction circuit comprises an amplifier having a variable gain or an attenuator having a variable attenuation (Yamazaki: column 3, lines 20-31), so that the difference between the levels of the right and left-eye video signals is corrected by adjusting said gain and attenuation depending upon the output level of said video signal correction circuit (Yamazaki: column 3, lines 40-50), as in the claim.

Regarding claims 14-15, Yamazaki discloses that said stereoscopic video signal processing circuitry is characterized in that said video signal correction circuit includes a level shift circuit which is capable of shifting the direct current level of an input signal (Yamazaki: column 2, lines 60-67: luminance level is DC level in an image), so that the difference between the levels of the right and left-eye video signals is corrected by adjusting the direct current level

of said input signal depending upon the direct current level of the output signal of said video signal correction circuit (Yamazaki: column 3, lines 19-30), as in the claim.

Regarding claim 16, Yamazaki discloses that said stereoscopic video signal processing circuitry is characterized in that said video signal correction circuit comprises a color correction circuit, which is capable of adjusting the tonality of the video signal to correct the difference between the tonality of the right and left-eye video signals (Yamazaki: column 3, lines 30-37), as in the claim.

Regarding claim 17, Yamazaki discloses that said stereoscopic video signal processing circuitry is characterized in that said video signal correction circuit operates to cause said first switch to pass one of the right and left-eye video signals and operates to alternately switch said second switch (Yamazaki: column 5, lines 30-50; figure 2, elements S7 and S8), as in the claim.

Conclusion

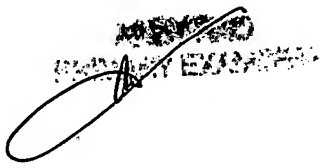
4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Lipton discloses a stereoscopic television system with field storage for sequential display of right and left images, a stereoscopic video camera, a stereoscopic television system, and a camera controller for a stereoscopic video system. Ohmura discloses an image photography apparatus with stereoscopic video.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy S. Rao whose telephone number is (571)-272-7337. The examiner can normally be reached on Monday-Friday 8 hours.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mehrdad Dastouri can be reached on (571)-272-7418. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Andy S. Rao
Primary Examiner
Art Unit 2621



asr
August 16, 2007